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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/702,372	11/05/2003	Ming-Dou Ker	JC-7897-DIV	8473

23900 7590 02/02/2006

J C PATENTS, INC.
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IRVINE, CA 92618

EXAMINER	
STARK, JARRETT J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/702,372	KER ET AL.	
	Examiner	Art Unit	
	Jarrett J. Stark	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *39-42 and 46-50* is/are pending in the application.

4a) Of the above claim(s) *40-42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *39 and 46-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 1/26/2006 have been fully considered but they are not persuasive.

Regarding claims 39 & 46, the applicant argues that Voldman et al. does not disclose the well. The examiner points out to the applicant that Figs. 2,4, & 7 and the front page of US Patent 6,015,993 all show the well. Voldman et al. Col. 4, lines 20-25 states:

"a lateral unidirectional bipolar type insulated gate transistor is formed in an implanted well 152 in a surface semiconductor layer 154."

United States Patent [19]
Voldman et al.

[11] **Patent Number: 6,015,993**
[45] **Date of Patent: Jan. 18, 2000**

[54] **SEMICONDUCTOR DIODE WITH DEPLETED POLYSILICON GATE STRUCTURE AND METHOD**

[75] Inventors: **Steven H. Voldman**, South Burlington; **Robert J. Gauthier, Jr.**, Hinesburg; **Jeffrey S. Brown**, Middlesex, all of Vt.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: 09/144,386

[22] Filed: Aug. 31, 1998

[51] Int. Cl.[7] H01L 23/62; H01L 29/76; H01L 29/00

[52] U.S. Cl. 257/355; 257/356; 257/339; 257/328; 257/546

[58] Field of Search 257/367, 373, 257/570, 328, 339, 440, 546, 551, 577, 355–363, 173

[56] References Cited

U.S. PATENT DOCUMENTS

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4,516,223	5/1985	Erickson .	
4,616,404	10/1986	Wang et al. .	
4,760,433	7/1988	Young et al.	257/357
4,760,434	7/1988	Tsuzuki et al. .	
4,896,199	1/1990	Tsuzuki et al. .	
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5,227,655	7/1993	Kayama .	
5,365,099	11/1994	Phipps et al. .	
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5,502,338	3/1996	Suda et al. .	
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5,629,544	5/1997	Voldman et al. .	
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FOREIGN PATENT DOCUMENTS

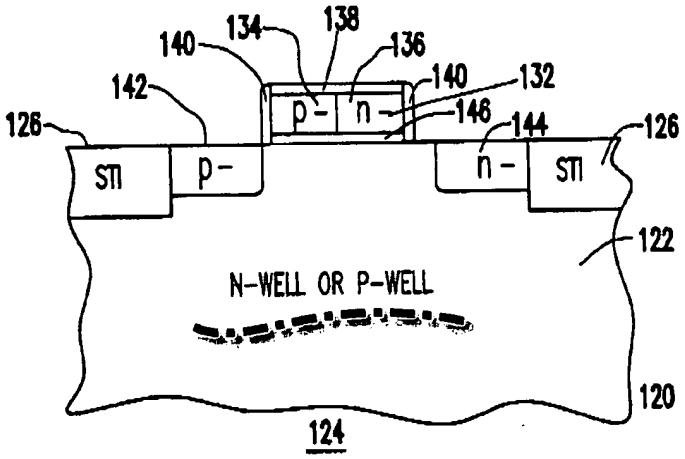
401185971	7/1989	Japan	257/355

Primary Examiner—Tom Thomas
Assistant Examiner—Ori Nadav
Attorney, Agent, or Firm—Whitham, Curtis & Whitham; Eugene I. Shkurko

[57] ABSTRACT

A high voltage tolerant diode structure for mixed-voltage, and mixed signal and analog/digital applications. The preferred silicon diode includes a polysilicon gate structure on at least one dielectric film layer on a semiconductor (silicon) layer or body. A well or an implanted area is formed in a bulk semiconductor substrate or in a surface silicon layer on an SOI wafer. Voltage applied to the polysilicon gate film, electrically depletes it, reducing voltage stress across the dielectric film. An intrinsic polysilicon film may be counter-doped, implanted with a low doped implantation, implanted with a low doped source/drain implant, or with a low doped MOSFET LDD or extension implant. Alternatively, a block mask may be formed over the gate structure when defining the depleted-polysilicon gate silicon diode to form low series resistance diode implants, preventing over-doping the film. Optionally, a hybrid photoresist method may be used to form higher doped edge implants in the silicon to reduce diode series resistance without a block mask.

15 Claims, 15 Drawing Sheets



For these reasons the applicant's arguments with respect to claims 39 & 46 have been considered but are moot.

Claim Objections

Claim 39 is objected to because of the following informalities: "and the N-type **heave**[SP?] doped region". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 39 is rejected under 35 U.S.C. 102(b) as being anticipated by Voldman et al. (US 6,015,993).

Regarding claim 39, Voldman teaches a method of forming a non-gate diode of a SOI, comprising:

providing an SOI with a substrate (Voldman, Figs. 7), an insulating layer (Voldman, Figs. 7, element 156) and a silicon layer (Voldman, Figs. 7, element 154) sequentially stacked together,

forming a pair of isolating structures (Voldman, Fig. 7, elements 126) in the silicon layer, so as to define a well region (Voldman, Fig. 7, elements 152) there between;

forming a lightly doped region in the well region, the lightly doped region comprising two neighboring lightly doped _-type region and N-type regions; and

forming a P-type heavily doped region and an N-type heavily doped region in the well region and wherein

the P-type heavily doped region (Fig. 7 [162]) is configured between and connects the lightly doped P-type region (Fig. 7 [142]) and one isolating structure(Fig. 7 [126]), and the N-type **heave**[SP?] doped region (Fig. 7 [164]) is configured between and connects the lightly doped N-type (Fig. 7 [144]) and the other isolating structure (Fig. 7 [126]).

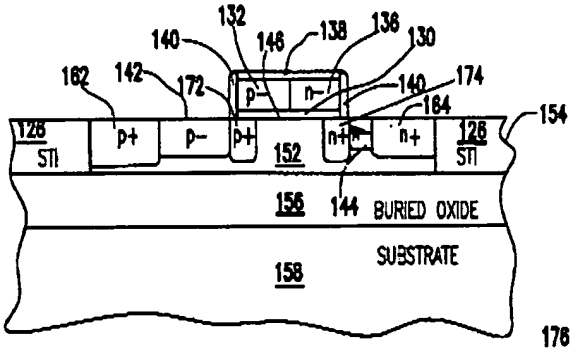


FIG.7

Regarding claim 40, Voldaman teaches the method according to claim 39, wherin the first type and second type doped regions are implanted with P-type and N-type ions, respectively (Voldaman, Fig. 7, elements 162 & 164).

Regarding claim 41, Voldaman teaches the method according to claim 39, wherein the well region is lightly implanted with a P-type ion (Voldaman, Fig. 7, elements 142).

Regarding claim 42, Voldaman teaches the method according to claim 39, wherein the well region is lightly implanted with an N-type ion (Voldaman, Fig. 7, elements 144).

Regarding claim 46, Voldaman teaches a method of forming a non-gate diode in a CMOS process, comprising:

Providing a substrate (Voldaman, Fig. 7, elements 156) having a well region therein (Voldaman, Fig. 7, elements 152);

Forming a pair of blocking isolation structures in the substrate (Voldaman, Fig. 7, elements 126);

Forming a first type-doped region (Voldaman, Fig. 7, elements 162) located in the well region and between the blocking isolation structure, and

Forming a pair of second type doped regions (Voldaman, Fig. 7, elements 144 & 164) located in the well region and respectively adjacent to the blocking isolation structure (Voldaman, Fig. 7, elements 126), wherein each second type doped region is separated from the first type doped region by the well (Voldaman, Fig. 7, elements 152).

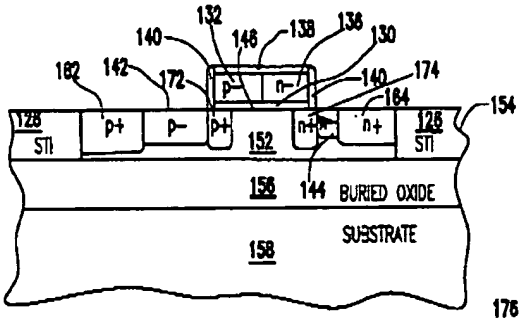


FIG.7

Regarding claim 47, Voldaman teaches the method according to claim 46, wherin the first type doped region and the second type doped region are implanted with P-type and N-type ions respectively (Voldaman, Fig. 7, elements 162 & 164).

Regarding claim 48, Voldaman teaches method according to claim 46, wherein the well region is lightly implanted with a P-type ion (Voldaman, Fig. 7, elements 142).

Regarding claim 49, Voldaman teaches method according to claim 46, wherein each second type doped region and the first type doped region defines a spacing, separating the second type doped region from the first type doped region (Voldaman, Fig. 7, elements 152).

Regarding claim 49, Voldaman teaches method according to claim 46, wherein the spacing is undoped. (Voldaman, Fig. 7, elements 152).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jarrett J. Stark whose telephone number is (571) 272-6005. The examiner can normally be reached on Monday - Thursday 7:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJS
January 31, 2006

W. DAVID COLEMAN
PRIMARY EXAMINER